

**WHAT IS CLAIMED IS:**

- 1 1. A method for transmitting a "J" bit block of data from a first electronic unit to a  
2 second electronic unit over a signaling bus having "K" signaling conductors, where  
3 zero to "K-1" of the signaling conductors is faulty, the method comprising the steps  
4 of:  
5 identifying faulty and nonfaulty signaling conductors in the signaling bus;  
6 setting a fault status of the signaling conductors in the first electronic unit and in the  
7 second electronic unit, using information found by the step of identifying faulty and  
8 nonfaulty signaling conductors in the signaling bus;  
9 determining "F", the number of faulty signaling conductors in the signaling bus;  
10 determining "K-F", the number of nonfaulty signaling conductors in the signaling  
11 bus; and  
12 transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors  
13 using "J/(K-F)" beats, plus an additional beat if a remainder exists.
- 1 2. The method of claim 1, the step of transmitting further comprises the steps of:  
2 selecting a "K" bit group of data from the "J" bit block of data;  
3 transmitting, on a beat, "K-F" bits of the "K" bit group of data, using the "K-F"  
4 nonfaulty conductors;  
5 storing the "F" bits in the "K" bit group that cannot be transmitted, on the beat, due to  
6 the "F" faulty conductors in the signaling bus;  
7 repeating the above three steps until all "J" bits of the "J" bit block of data have been  
8 selected; and  
9 transmitting the stored "F" bits on one or more additional beats, using one or more  
10 of the "K-F" nonfaulty signaling conductors.
- 1 3. The method of claim 2, the step of storing the "F" bits further comprising the step of  
2 shifting at least one bit of the "F" bits into a first end of a shift register.
- 1 4. The method of claim 3, further comprising the step of transmitting at least one of the  
2 bits of the the shift register to a nonfaulty signaling conductor.

- 1 5. The method of claim 4, further comprising the step of moving a particular bit in the  
2 shift register to align that particular bit for coupling to a nonfaulty signaling  
3 conductor.
- 1 6. The method of claim 2, further comprising the steps of:  
2 storing, in the second electronic unit, "K-F" bits per beat for "J/(K-F)" beats; and  
3 storing remainder bits in an additional beat, if "J/(K-F)" results in a remainder.
- 1 7. The method of claim 1, further comprising the steps of:  
2 selecting a "K-F" bit group of bits from the "J" bit block of data on the first electronic  
3 unit;  
4 transmitting the "K-F" bit group of bits from the first electronic unit to the second  
5 electronic unit using the "K-F" nonfaulty signaling conductors in the signaling bus,  
6 using a beat of the signaling bus;  
7 repeating the previous steps until all "K-F" bit groups have been transmitted; and  
8 transmitting any remaining bits of the "J" bit block of data on the first electronic unit  
9 to the second electronic unit using some or all of the "K-F" nonfaulty signaling  
10 conductors, using an additional beat of the signaling bus.
- 1 8. An apparatus for transmitting a "J" bit block of data from a first electronic unit to a  
2 second electronic unit comprising:  
3 a first block of data in the first electronic unit holding "J" bits for transmission;  
4 storage in the second electronic capable of holding a second block of data having  
5 "J" bits;  
6 a signaling bus having "K" signaling conductors coupling the first electronic unit to  
7 the second electronic unit, the signaling bus having "F" faulty signaling conductors  
8 and "K-F" nonfaulty signaling conductors;  
9 a diagnostic unit coupled to the first electronic unit and to the second electronic unit  
10 capable of identifying the "F" faulty signaling conductors and the "K-F" nonfaulty  
11 signaling conductors on the signaling bus and storing fault identification information  
12 in the first electronic unit and in the second electronic unit; and

- 13 a driving sequencer in the first electronic unit that, respondent to the fault  
14 identification information, transmits the "J" bits of data using "J/(K-F)" beats, plus an  
15 additional beat if a remainder exists, using only the "K-F" nonfaulty conductors.
- 1 9. The apparatus of claim 8, the first block of data being selectable by select groups of  
2 "K" bits at a time.
- 1 10. The apparatus of claim 8, the driving sequencer capable of selecting "K-F" bits at a  
2 time from the first block of data, and driving the "K-F" selected bits onto the "K-F"  
3 nonfaulty signaling conductors of the signaling bus, the driving sequencer further  
4 capable of selecting fewer than "K-F" bits for an additional beat if "J/(K-F)" has a  
5 remainder.
- 1 11. The apparatus of claim 10, the driving sequencer further comprising drivers capable  
2 of being disabled; wherein the driving sequencer disables a driver coupled to a  
3 faulty signaling conductor.
- 1 12. The apparatus of claim 10, the second electronic unit further comprising a receiving  
2 sequencer coupled to the signaling bus and to the diagnostic unit, the receiving  
3 sequencer capable of storing "K-F" bits at a time into the second block of data, the  
4 "K-F" bits received from the "K-F" nonfaulty signaling conductors of the signaling  
5 bus, the receiving sequencer further capable of storing fewer than "K-F" bits if "J/(K-  
6 F)" has a remainder.
- 1 13. A method for transmitting a block of data from a first electronic unit to a second  
2 electronic unit over a signaling bus, comprising the steps of:  
3 identifying nonfaulty signaling conductors in the signaling bus; and  
4 transmitting the block of data using a transmission sequence from the first electronic  
5 unit to the second electronic unit, the transmission sequence utilizing all of the  
6 nonfaulty signaling conductors in the signaling bus;  
7 wherein the transmission sequence uses a minimum number of beats to complete  
8 the transmission of the block of data.
- 1 14. The method of claim 13, wherein the nonfaulty signaling conductors are identified  
2 during a power on sequence.

1 15. The method of claim 13, wherein the nonfaulty signaling conductors are identified by  
2 a wire test performed as a result of a parity error, and error correcting code error, or  
3 a cyclical redundancy check error.

1 16. The method of claim 13, further comprising the steps of:  
2 identifying a faulty signaling conductor in the signaling bus; and  
3 switching a driver coupled to the faulty signaling conductor to a high impedance  
4 state.